AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 37, 38, 40, 41 and 43 without prejudice or disclaimer.

Please **AMEND** claims 36, 39 and 42 as shown below.

The following is a complete list of all claims in this application.

1-35. (Cancelled)

36. (Currently Amended) An apparatus for manufacturing a liquid crystal device, comprising:

a ~~first~~ loading chamber receiving a substrate; ~~and~~

a preheat chamber receiving the substrate from the first chamber and preheating the substrate;

a ~~second~~ chemical vapor deposition (CVD) chamber receiving the substrate from the preheat chamber and forming a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer on the substrate; and

a ~~third~~ sputtering chamber receiving the substrate from the CVD chamber and forming a metal layer on the doped amorphous silicon layer,

wherein the loading chamber, the preheat chamber, the CVD chamber and the sputtering chamber are connected in series, and the apparatus sequentially forms the gate insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer without breaking a vacuum and without patterning the gate

insulating layer, the amorphous silicon layer, the doped amorphous silicon layer and the metal layer.

37-38. (Cancelled)

39. (Currently Amended) The apparatus of claim 36, wherein the ~~first~~ loading chamber receives the substrate having a gate line formed thereon.

40-41. (Cancelled)

42. (Currently Amended) The apparatus of claim 36, wherein the ~~second~~ CVD chamber comprises:

a first ~~deposition~~ CVD chamber forming the gate insulating layer and an amorphous silicon layer; and

a second ~~deposition~~ CVD chamber forming the doped amorphous silicon layer.

43. (Cancelled)

44. (Previously Presented) The apparatus of claim 36, wherein the metal layer is chromium.

45. (Previously Presented) The apparatus of claim 36, wherein the gate insulating layer is formed at a thickness between 3000 Å to 6000 Å, the amorphous

silicon layer is formed at a thickness between 1000 Å to 3000 Å, and the doped amorphous silicon layer is formed at a thickness of 200 Å to 1000 Å.